WHAT IS CLAIMED IS

1. A solid-state image sensor comprising:

a plurality of pixel units arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter, a first transistor for transferring a signal generated by the photoelectric converter, a second transistor for amplifying the signal, a third transistor for resetting an input terminal of the second transistor, and a fourth transistor for reading the signal outputted by the second transistor;

a plurality of first signal lines extended in the row direction, each of the first signal lines being connected to gate electrodes of the first transistors of the pixel units arranged in the row direction; and

a plurality of second signal lines extended in the row direction, each of the second signal lines being connected to gate electrodes of the fourth transistors of the pixel units arranged in the row direction,

the first signal line connected to the gate electrodes of the first transistors of the pixel units of an n^{th} row, and the second signal line connected to the gate electrodes of the fourth transistors of the pixel units of an $n+1^{th}$ row being formed of a common signal line, and

in each pairs of the pixel units of the n^{th} row and the $n+1^{th}$ row corresponding to each other, the gate electrode of the first transistor of the pixel unit of the n^{th} row and

the gate electrode of the fourth transistor of the pixel unit of the n+1th row being formed in one continuous pattern of the same conducting layer.

2. A solid-state image sensor according to claim 1, further comprising:

a plurality of third signal lines extended in the row direction, each of the third signal lines being connected to gate electrodes of the third transistors of the pixel units arranged in the row direction;

a plurality of fourth signal lines extended in the column direction, each of the fourth signal lines being for applying a reset voltage to the second transistors and the third transistors of the of pixel units arranged in the column direction; and

a plurality of fifth signal lines extended in the column direction, each of the fifth signal lines being for reading the signals from the fourth transistors of the pixel units arranged in the column direction,

the common signal lines of the first signal lines and the second signal lines being formed of a first metal interconnection layer,

the third signal lines being formed of a second metal interconnection layer,

the fourth signal lines and the fifth signal lines being formed of a third metal interconnection layer.

3. A solid-state image sensor according to claim 1,

wherein

the first signal line connected to the pixel units of the n^{th} row, and the second signal line connected to the pixel units of the $n+1^{th}$ row, the gate electrodes of the first transistors of the pixels of the n^{th} row and the gate electrodes of the fourth transistors of the $n+1^{th}$ row are formed in one continuous pattern of said conducting layer.

4. A solid-state image sensor according to claim 3, further comprising:

a plurality of third signal lines extended in the row direction, each of the third signal lines being connected to gate electrodes of the third transistors of the pixel units arranged in the row direction;

a plurality of fourth signal lines extended in the column direction, each of the fourth signal lines being for applying a reset voltage to the second transistors and the third transistors of the of pixel units arranged in the column direction; and

a plurality of fifth signal lines extended in the column direction, each of the fifth signal lines being for reading the signals from the fourth transistors of the pixel units arranged in the column direction,

the third signal lines being formed of a first metal interconnection layer, and

the fourth signal lines and the fifth signal lines being formed of a second metal interconnection layer.

5. A solid-state image sensor according to claim 1, wherein

the photoelectric converter and the first transistor are adjacent to each other in the row direction,

the second transistor and the third transistor are adjacent to each other in the column direction, and

the gate electrode of the first transistor and the gate electrode of the fourth transistor are extended in the column direction.

6. A solid-state image sensor comprising:

a plurality of pixel units arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter, a first transistor for transferring a signal generated by the photoelectric converter, a second transistor for amplifying the signal, a third transistor for resetting an input terminal of the second transistor, and a fourth transistor for reading the signal outputted by the second transistor;

a plurality of first signal lines extended in the row direction, each of the first signal lines being connected to gate electrodes of the third transistors of the pixel units arranged in the row direction; and

a plurality of second signal lines extended in the row direction, each of the second signal lines being connected to gate electrodes of the fourth transistors of the pixel units arranged in the row direction,

the first signal line connected to the gate electrodes of the third transistors of the pixel units of an n^{th} row, and the second signal line connected to the gate electrodes of the fourth transistors of the pixel units of an $n+1^{th}$ row being formed of a common signal line, and

in each pairs of the pixel units of the n^{th} row and the $n+1^{th}$ row corresponding to each other, the gate electrode of the third transistor of the pixel unit of the n^{th} row and the gate electrode of the fourth transistor of the pixel unit of the $n+1^{th}$ row being formed in one continuous pattern of the same conducting layer.

7. A solid-state image sensor according to claim 6, further comprising:

a plurality of third signal lines extended in the row direction, each of the third signal lines being connected to gate electrodes of the first transistors of the pixel units arranged in the row direction;

a plurality of fourth signal lines extended in the column direction, each of the fourth signal lines being for applying a reset voltage to the second transistors and the third transistors of the of pixel units arranged in the column direction; and

a plurality of fifth signal lines extended in the column direction, each of the fifth signal lines being for reading the signals from the fourth transistors of the pixel units arranged in the column direction,

the common signal lines of the first signal lines and the second signal lines being formed of a first metal interconnection layer,

the fourth signal lines and the fifth signal lines being formed of a second metal interconnection layer,

the third signal lines being formed of a third metal interconnection layer.

8. A solid-state image sensor according to claim 6, wherein

the first signal line connected to the pixel units of the n^{th} row, and the second signal line connected to the pixel units of the $n+1^{th}$ row, the gate electrodes of the third transistors of the pixels of the n^{th} row and the gate electrodes of the fourth transistors of the $n+1^{th}$ row are formed in one continuous pattern of said conducting layer.

9. A solid-state image sensor according to claim 8, further comprising:

a plurality of third signal lines extended in the row direction, each of the third signal lines being connected to gate electrodes of the first transistors of the pixel units arranged in the row direction;

a plurality of fourth signal lines extended in the column direction, each of the fourth signal lines being for applying a reset voltage to the second transistors and the third transistors of the of pixel units arranged in the column direction; and

a plurality of fifth signal lines extended in the column direction, each of the fifth signal lines being for reading the signals from the fourth transistors of the pixel units arranged in the column direction,

the third signal lines being formed of a first metal interconnection layer,

the fourth signal lines and the fifth signal lines being formed of a second metal interconnection layer.

10. A solid-state image sensor according to claim 1, wherein

the photoelectric converter and the first transistor are adjacent to each other in the column direction,

the second transistor, the third transistor, and the fourth transistor are adjacent to each other in the column direction, and

the gate electrode of the first transistors, the gate electrodes of the second transistors, the gate electrodes of the third transistors, and the gate electrodes of the fourth transistors are extended in the row direction.

11. A solid-state image sensor according to claim 6, wherein

the photoelectric converter and the first transistor are adjacent to each other in the column direction,

the second transistor, the third transistor, and the fourth transistor are adjacent to each other in the column direction, and

the gate electrode of the first transistors, the gate electrodes of the second transistors, the gate electrodes of the third transistors, and the gate electrodes of the fourth transistors are extended in the row direction.

12. A solid-state image sensor according to claim 10, wherein

a first region where the photoelectric converter and the first transistor are formed, and a second region where the second to the fourth transistors are formed are adjacent to each other in the row direction.

13. A solid-state image sensor according to claim 11, wherein

a first region where the photoelectric converter and the first transistor are formed, and a second region where the second to the fourth transistors are formed are adjacent to each other in the row direction.

14. A solid-state image sensor according to claim 10, wherein

a first region where the photoelectric converter and the first transistor are formed, and a second region where the second to the fourth transistors are formed are relatively diagonally adjacent to each other.

15. A solid-state image sensor according to claim 11, wherein

a first region where the photoelectric converter and the first transistor are formed, and a second region where

the second to the fourth transistors are formed are relatively diagonally adjacent to each other.

16. A solid-state image sensor according to claim 10, further comprising:

an active region where a drain region of the first transistor and a source region of the third transistor has a pattern elongated in the row direction.

17. A solid-state image sensor according to claim 11, further comprising:

an active region where a drain region of the first transistor and a source region of the third transistor has a pattern elongated in the row direction.

18. A solid-state image sensor comprising:

a plurality of pixel units arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter, a first transistor for transferring a signal generated by the photoelectric converter, a second transistor for amplifying the signal, a third transistor for resetting an input terminal of the second transistor, and a fourth transistor for reading the signal outputted by the second transistor;

a plurality of first signal lines extended in the row direction, each of the first signal lines being connected to gate electrodes of the first transistors of the pixel units arranged in the row direction; and

a plurality of second signal lines extended in the row

direction, each of the second signal lines being connected to gate electrodes of the third transistors of the pixel units arranged in the row direction,

the first signal line connected to the gate electrodes of the first transistors of the pixel units of an n^{th} row, and the second signal line connected to the gate electrodes of the third transistors of the pixel units of an $n+1^{th}$ row being formed of a common signal line, and

in each pairs of the pixel units of the n^{th} row and the $n+1^{th}$ row corresponding to each other, the gate electrode of the first transistor of the pixel unit of the n^{th} row and the gate electrode of the third transistor of the pixel unit of the $n+1^{th}$ row being formed in one continuous pattern of the same conducting layer.

19. A solid-state image sensor according to claim 18, wherein

the photoelectric converter and the first transistor are adjacent to each other in the row direction,

the second transistor, the third transistor, and the fourth transistors are adjacent to one another in the row direction, and

the gate electrode of the first transistor, the gate electrode of the second transistor, the gate electrode of the third transistor, and the gate electrode of the fourth transistor are extended in the column direction.

20. A solid-state image sensor according to claim 18,

further comprising:

a plurality of third signal lines extended in the row direction, each of the third signal lines being connected to gate electrodes of the fourth transistors of the pixel units arranged in the row direction;

a plurality of fourth signal lines extended in the column direction, each of the fourth signal lines being for applying a reset voltage to the second transistors and the third transistors of the of pixel units arranged in the column direction; and

a plurality of fifth signal lines extended in the column direction, each of the fifth signal lines being for reading the signals from the fourth transistors of the pixel units arranged in the column direction,

the fourth signal lines and the fifth signal lines being forming of a first metal interconnection layer, and

the common signal lines of the first signal lines and the second signal lines, and the third signal lines are formed of a second metal interconnection layer.

21. A solid-state image sensor according to claim 4, further comprising

a light shield film formed of a third metal interconnection layer.

22. A solid-state image sensor according to claim 9, further comprising

a light shield film formed of a third metal interconnection

layer.

23. A solid-state image sensor according to claim 20, further comprising

a light shield film formed of a third metal interconnection layer.

24. A solid-state image sensor according to claim 1, further comprising:

a metal interconnection interconnecting a source terminal of the third transistor and a gate terminal of the second transistor, the metal interconnection having a width which is selectively increased in a region above a drain region of the first transistor and the a source region of the third transistor.

25. A solid-state image sensor according to claim 6, further comprising:

a metal interconnection interconnecting a source terminal of the third transistor and a gate terminal of the second transistor, the metal interconnection having a width which is selectively increased in a region above a drain region of the first transistor and the a source region of the third transistor.

26. A solid-state image sensor according to claim 18, further comprising:

a metal interconnection interconnecting a source terminal of the third transistor and a gate terminal of the second transistor, the metal interconnection having a width which

is selectively increased in a region above a drain region of the first transistor and the a source region of the third transistor.

27. A solid-state image sensor comprising: a plurality of pixel units arranged in a row direction and a column direction,

each of the plurality of pixel units including a photoelectric converter, a first transistor for transferring a signal generated by the photoelectric converter, a second transistor for amplifying the signal, a third transistor for resetting an input terminal of the second transistor, and a fourth transistor for reading the signal outputted by the second transistor,

the photoelectric converter and the first transistor being adjacent to each other in the column direction,

the second transistor, the third transistor, and the fourth transistor being adjacent to each other in the column direction,

a gate electrode of the first transistor, a gate electrode of the second transistor, a gate electrode of the third transistor, and a gate electrode of the fourth transistor being extended in the row direction, and

a first region where the photoelectric converter and the first transistor are formed, and a second region where the second to the fourth transistors are formed are relatively diagonally adjacent to each other.

28. A solid-state image sensor according to claim 1, wherein

a contact hole opened onto a source region of the third transistor, and a contact hole opened onto a drain region of the third transistor and/or a contact hole opened onto a source region of the fourth transistor are formed by self-alignment with the gate electrode.

29. A solid-state image sensor according to claim 6, wherein

a contact hole opened onto a source region of the third transistor, and a contact hole opened onto a drain region of the third transistor and/or a contact hole opened onto a source region of the fourth transistor are formed by self-alignment with the gate electrode.

30. A solid-state image sensor according to claim 18, wherein

a contact hole opened onto a source region of the third transistor, and a contact hole opened onto a drain region of the third transistor and/or a contact hole opened onto a source region of the fourth transistor are formed by self-alignment with the gate electrode.

31. A solid-state image sensor according to claim 27, wherein

a contact hole opened onto a source region of the third transistor, and a contact hole opened onto a drain region of the third transistor and/or a contact hole opened onto

a source region of the fourth transistor are formed by self-alignment with the gate electrode.

32. A solid-state image sensor according to claim 1, wherein

in a pixel of the n^{th} row and a pixel of the $n+1^{th}$ row which are positioned diagonally to each other, the gate electrode of the first transistor of the pixel of the n^{th} row and the gate electrode of the fourth transistor of the pixel of the $n+1^{th}$ row are formed in one continuous pattern of said conducting layer.

33. An image reading method for a solid-state image sensor comprising: a plurality of pixel units arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter, a first transistor for transferring a signal generated by the photoelectric converter, a second transistor for amplifying the signal, a third transistor for resetting an input terminal of the second transistor, and a fourth transistor for reading the signal outputted by the second transistor; a plurality of first signal lines extended in the row direction, each of the first signal lines being connected to gate electrodes of the first transistors of the pixel units arranged in the row direction; and a plurality of second signal lines extended in the row direction, each of the second signal lines being connected to gate electrodes of the fourth transistors of the pixel units arranged in the row direction, the first signal

line connected to the gate electrodes of the first transistors of the pixel units of an n^{th} row, and the second signal line connected to the gate electrodes of the fourth transistors of the pixel units of an $n+1^{th}$ row being formed of a common signal line, the method comprising the steps of:

globally resetting the photoelectric converters and the second transistors in all the rows;

after a period of a photo detection time, globally transferring charges from the photoelectric converters to the gate terminals of the second transistors via the first transistors in all the rows; and

reading signals and reading reset voltages in each of the rows.

34. An image reading method for a solid-state image sensor comprising: a plurality of pixel units arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter, a first transistor for transferring a signal generated by the photoelectric converter, a second transistor for amplifying the signal, a third transistor for resetting an input terminal of the second transistor, and a fourth transistor for reading the signal outputted by the second transistor; a plurality of first signal lines extended in the row direction, each of the first signal lines being connected to gate electrodes of the third transistors of the pixel units arranged in the row direction; and a plurality of second signal lines extended

in the row direction, each of the second signal lines being connected to gate electrodes of the fourth transistors of the pixel units arranged in the row direction, the first signal line connected to the gate electrodes of the third transistors of the pixel units of an n^{th} row, and the second signal line connected to the gate electrodes of the fourth transistors of the pixel units of an $n+1^{th}$ row being formed of a common signal line, the method comprising the steps of:

globally resetting the photoelectric converters and the second transistors in all the rows;

after a period of a photo detection time, globally transferring charges from the photoelectric converters to the gate terminals of the second transistors via the first transistors in all the rows; and

reading signals and reading reset voltages in each of the rows.

35. An image reading method for a solid-state image sensor comprising: a plurality of pixel units arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter, a first transistor for transferring a signal generated by the photoelectric converter, a second transistor for amplifying the signal, a third transistor for resetting an input terminal of the second transistor, and a fourth transistor for reading the signal outputted by the second transistor; a plurality of first signal lines extended in the row direction, each

of the first signal lines being connected to gate electrodes of the third transistors of the pixel units arranged in the row direction; and a plurality of second signal lines extended in the row direction, each of the second signal lines being connected to gate electrodes of the fourth transistors of the pixel units arranged in the row direction, the first signal line connected to the gate electrodes of the third transistors of the pixel units of an n^{th} row, and the second signal line connected to the gate electrodes of the fourth transistors of the pixel units of an $n+1^{th}$ row being formed of a common signal line, the method comprising the steps of:

globally resetting the photoelectric converters and the second transistors at first reset voltages in all the rows;

after a period of a photo detection time, globally transferring charges from the photoelectric converters to the gate terminals of the second transistors via the first transistors in all the rows; and

reading signals and reading second reset voltages which are higher than the first reset voltage in each of the rows.

36. An image reading method according to claim 33, wherein

the step of resetting the photoelectric converter and the second transistors and the step of transferring charges to the gate terminals of the second transistors are performed with signal read lines shut off from peripheral circuits.

37. An image reading method according to claim 34,

wherein

the step of resetting the photoelectric converter and the second transistors and the step of transferring charges to the gate terminals of the second transistors are performed with signal read lines shut off from peripheral circuits.

38. An image reading method according to claim 35, wherein

the step of resetting the photoelectric converter and the second transistors and the step of transferring charges to the gate terminals of the second transistors are performed with signal read lines shut off from peripheral circuits.